

DIGITAL CLOCK WITH MULTIPLE SELECTIONS

Digital Clock with Multiple Selections

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Introduction

The purpose of this project is to understand and apply techniques taught in EE 210 to design a solution. The problem that was chosen is to design a digital clock with format selection. Designing this will show the significance of using the techniques in an industrial environment and can be implemented in real life without budgetary issues. The design will allow the user to change the hour hand format from standard to military time and vice versa at any given moment. In addition, the user will have the option to pause/resume the clock and set the time as well as weekdays. The most challenging part of this design is allowing the user to change the format and create most logic devices from scratch. The software that will be used to simulate the design is Logisim as it allows the designer to use its combinational analysis feature to generate Boolean functions given a truth table. This will certainly decrease the unnecessary time for computing large amounts of functions.

Methods

The first part of this project is to design the counters for each hand (seconds, minute, hour). Since the ranges for the second and hour hand are the same (0-59), both hands can use the same counters. The seconds-hand will consist of 2 counters for two 7-segment LED displays. The first counter will count from 0-9 and the second from 0-5. All the counters in this project will use leading edge-triggered JK Flip Flops due to their quicker design process. Each counter circuit will be synchronous, meaning all the clock input in the flip flops will be connected to a single clock. Because the first digit goes up to 9, we will need to list all possible variations of a 4-bit number in order and lists its next states respectively. The J and K inputs for each next state can be directly found using the quick method (Only applicable to D and JK flip flops) by separating the Karnaugh maps of each state into two maps (Note: the work for each counter can be found in attached PDF titled 'Project Work') After implanting into Logisim:

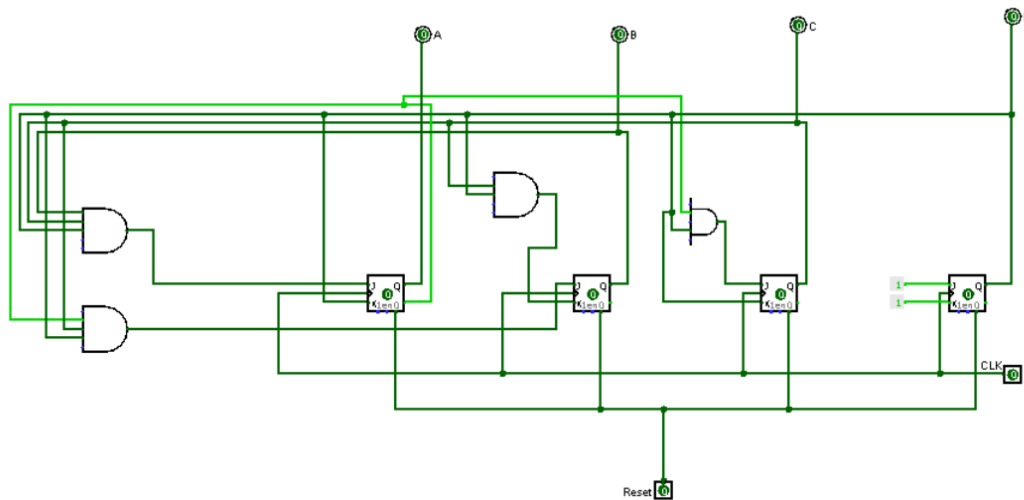


Figure 1: 0-9 up counter design

All the counters have a clock and reset as inputs. We can modify the counter to count up to a certain value using the reset feature.

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Now that the decoder is available, we can connect the displays and counters:

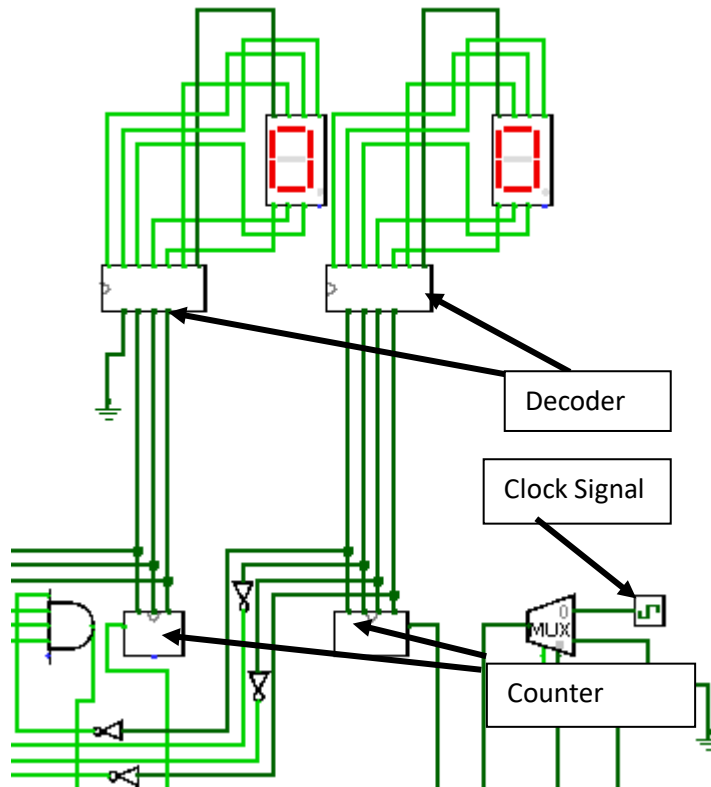


Figure 4: Seconds section of the digital clock

The clock signal is connected to a 2:1 multiplexer at the input position 0. This will allow the user to pause the clock with the selector line, with 1 being paused as position 1 is connected to the ground.

All the outputs in the first counter are inverted and connected with an AND gate, which is connected to the second counter. The outputs of the second counter are connected to the clock input of the first counter of the minute hand with an AND gate, and so on. The minute hand is essentially the same as the second-hand, except its clock inputs:

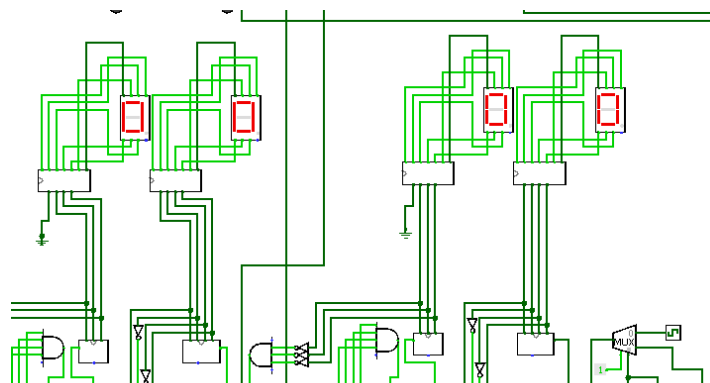


Figure 5: Minute Hand (left) and Seconds Hand (right)

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The hour hands will be different from that of the others because it resets differently. To decrease the use of multiple counters, the counter will count to multiple digits, from 1 to 12.

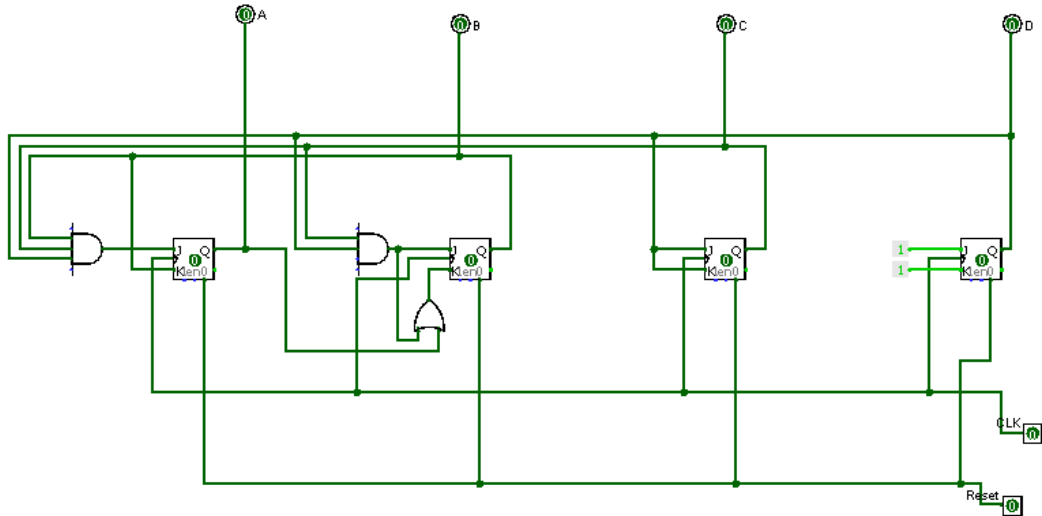


Figure 6: 12-hour counter

Since there needs to be a selection between standard and military time, another counter (0-24) will need to be designed with 5 flip flops:

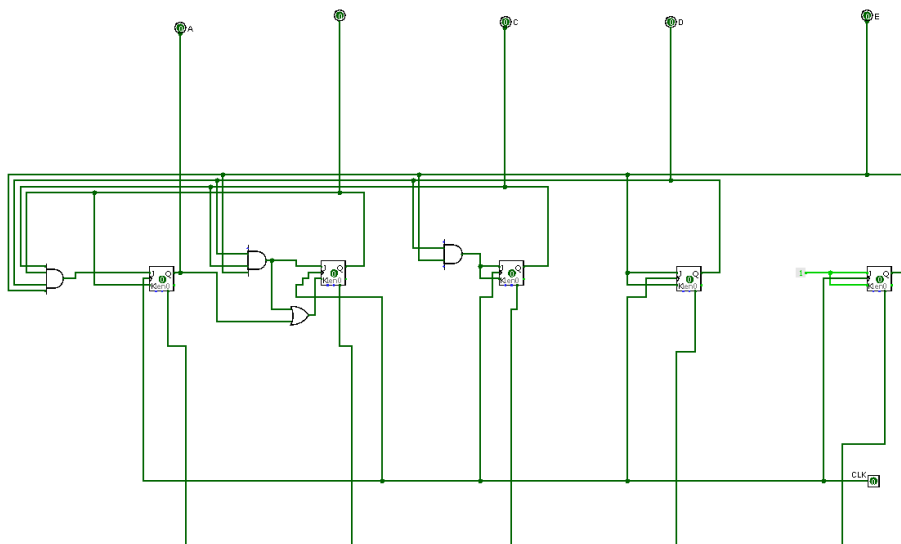


Figure 7: 24 hour counter

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The two counters will be connected to the same clock and run in parallel. 5 2:1 multiplexers will be used to allow the users to select the formats.

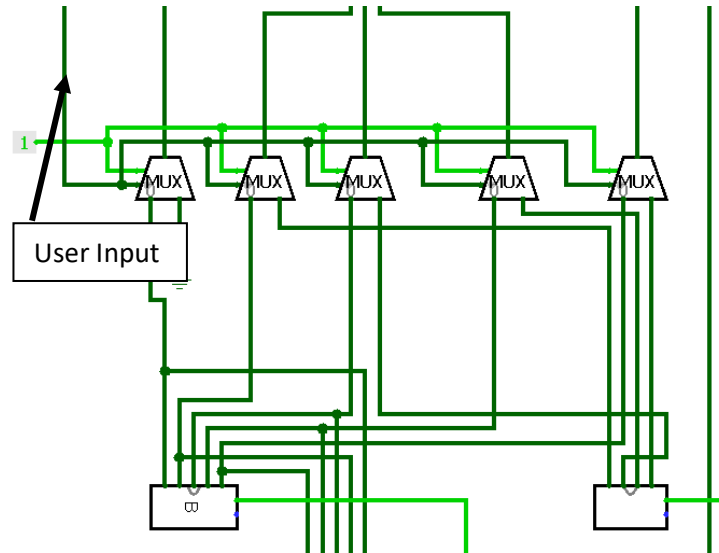


Figure 8: Format Selector

The 2 data inputs in each multiplexer are connected to the corresponding outputs of counters (Left 24-hour and right 12-hour). The selectors are connected and then to a toggle button where switching to 1 changes to the 12-hour format.

The decoders for the hour hand counters are also different since the other one cannot decode multiple digits. The first decoder outputs the first digit of a number. It was designed with the truth table as follows:

A	B	C	D	E	a1	b1	c1	d1	e1	f1	g1
0	0	0	0	0	1	1	1	1	1	1	0
0	0	0	0	1	0	1	1	0	0	0	0
0	0	0	1	0	1	1	0	1	1	0	1
0	0	0	1	1	1	1	1	1	0	0	1
0	0	1	0	0	0	1	1	0	0	1	1
0	0	1	0	1	1	0	1	1	0	1	1
0	0	1	1	0	1	0	1	1	1	1	1
0	0	1	1	1	1	1	1	0	0	0	0
0	1	0	0	0	1	1	1	1	1	1	1
0	1	0	0	1	1	1	1	1	0	1	1
0	1	0	1	0	1	1	1	1	1	1	0
0	1	0	1	1	0	1	1	0	0	0	0
0	1	1	0	0	1	1	0	1	1	0	1
0	1	1	0	1	1	1	1	1	0	0	1
0	1	1	1	0	0	1	1	0	0	1	1
0	1	1	1	1	1	0	1	1	0	1	1
1	0	0	0	0	1	0	1	1	1	1	1
1	0	0	0	1	1	1	1	0	0	0	0
1	0	0	1	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	1	0	1	1
1	0	1	0	0	1	1	1	1	1	1	0
1	0	1	0	1	0	1	1	0	0	0	0
1	0	1	1	0	1	1	0	1	1	0	1
1	0	1	1	1	1	1	1	1	0	0	1
1	1	0	0	0	0	1	1	0	0	1	1
1	1	0	0	1	1	0	1	1	0	1	1
1	1	0	1	0	1	0	1	1	1	1	1
1	1	0	1	1	1	1	1	0	0	0	0
1	1	1	0	0	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	0	1	1
1	1	1	1	0	1	1	1	1	1	1	0
1	1	1	1	1	0	1	1	0	0	0	0

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Figure 9: Truth table for the first digit of the hour-hand

The second digit decoder:

A	B	C	D	E	a2	b2	c2	d2	e2	f2	g2
0	0	0	0	0	1	1	1	1	1	1	0
0	0	0	0	1	1	1	1	1	1	1	0
0	0	0	1	0	1	1	1	1	1	1	0
0	0	0	1	1	1	1	1	1	1	1	0
0	0	1	0	0	1	1	1	1	1	1	0
0	0	1	0	1	1	1	1	1	1	1	0
0	0	1	1	0	1	1	1	1	1	1	0
0	0	1	1	1	1	1	1	1	1	1	0
0	1	0	0	0	1	1	1	1	1	1	0
0	1	0	0	1	1	1	1	1	1	1	0
0	1	0	1	0	0	1	1	0	0	0	0
0	1	0	1	1	0	1	1	0	0	0	0
0	1	1	0	0	0	1	1	0	0	0	0
0	1	1	0	1	0	1	1	0	0	0	0
0	1	1	1	0	0	1	1	0	0	0	0
0	1	1	1	1	0	1	1	0	0	0	0
1	0	0	0	0	0	1	1	0	0	0	0
1	0	0	0	1	0	1	1	0	0	0	0
1	0	0	1	0	0	1	1	0	0	0	0
1	0	0	1	1	0	1	1	0	0	0	0
1	0	1	0	0	1	1	0	1	1	0	1
1	0	1	0	1	1	1	0	1	1	0	1
1	0	1	1	0	1	1	0	1	1	0	1
1	0	1	1	1	1	1	0	1	1	0	1
1	1	0	0	0	1	1	0	1	1	0	1
1	1	0	0	1	1	1	0	1	1	0	1
1	1	0	1	0	1	1	0	1	1	0	1
1	1	0	1	1	1	1	0	1	1	0	1
1	1	1	0	0	1	1	0	1	1	0	1
1	1	1	0	1	1	1	0	1	1	0	1
1	1	1	1	0	1	1	0	1	1	0	1
1	1	1	1	1	1	1	1	0	0	0	1
1	1	1	1	1	1	1	1	1	0	0	1

Figure 10: Second digit decoder for the hour-hand

The second display changes its number every 10s digit. Now that the clock is complete, the next step is to create a weekday cycle that cycles from Monday to Sunday. We can reuse the 0-9 counter and modify it with the reset but so that it counts from 0-6. This means that the counter must reset when it changes to seven. The counter is triggered when the 24-hour counter resets to 0. The counter is then connected to a decoder to translate binary numbers to the day of the week. The truth table consists of 3 inputs and 7 outputs where there are descending 1s in a diagonal manner and 0s everywhere else. The resulting circuit:

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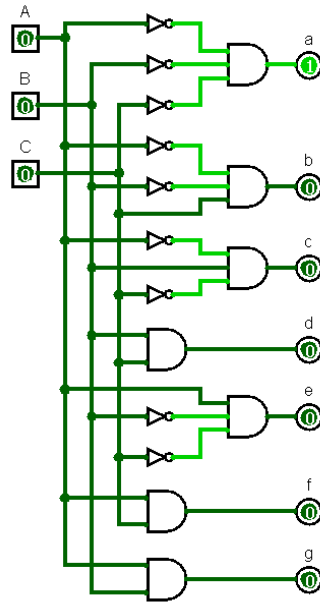


Figure 11: Weekday decoder

To give the user the ability to cycle through each section of the clock and set the desired time and day, we must design an 1 to 8 demultiplexer with the truth table:

EN	IN	s0	s1	s2	f0	f1	f2	f3	f4	f5	f6	f7
0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0	0	0	0
0	0	1	1	1	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	1	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0	0
0	1	0	1	1	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0	0
0	1	1	0	1	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	0	0
0	1	1	1	1	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0
1	0	1	0	1	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0
1	0	1	1	1	0	0	0	0	0	0	0	0
1	1	0	0	0	1	0	0	0	0	0	0	0
1	1	0	0	1	0	1	0	0	0	0	0	0
1	1	0	1	0	0	0	1	0	0	0	0	0
1	1	0	1	1	0	0	0	1	0	0	0	0
1	1	1	0	0	0	0	0	0	1	0	0	0
1	1	1	0	1	0	0	0	0	0	1	0	0
1	1	1	1	0	0	0	0	0	0	0	1	0
1	1	1	1	1	0	0	0	0	0	0	0	1

Figure 12: Truth table for 8:1 DMUX

In this table, all outputs are set to zero if enable (EN) is 0. If EN=1 and the user input (IN) = 1,

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the output will correspond to the values of the selector (s_0, s_1, s_2). The DMUX has 8 values since the selector is 3-bit. The demultiplexer will be enabled only if the user pauses the clock. To cycle through the outputs, the selector will be connected to a counter 0-5 counter because we will only have 6 options. The clock input of the counter is a button that the user presses to change selection. The input is also a button that will send an activation signal to the selected output. Each output of the DMUX is connected to the clock input of each counter connected to the digital clock through an XOR gate. This will let the user change the time without being affected by the sequential clock inputs. However, the user would not know which section is being selected. The solution is to use another 8 to 1 DMUX and counter with the same clock input as the other. The input in this will be an active 1 and the outputs will be connected to LEDs and placed in corresponding positions.

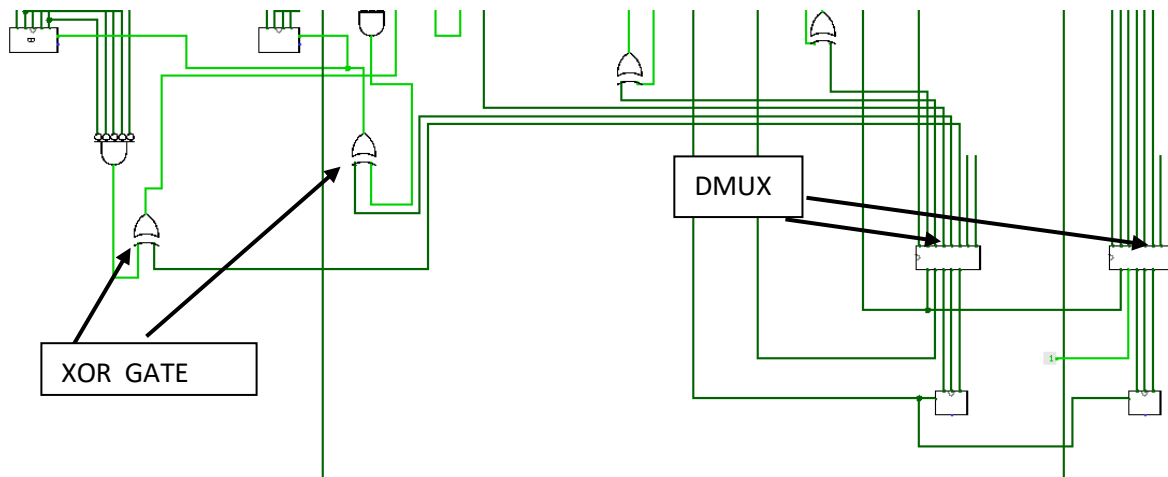


Figure 13: Selection System

Results

Before reading, please watch the video of the working simulation:

<https://www.youtube.com/watch?v=4VfC2mtiGLc&t=2s>

Using the logging tool in Logisim, we can now analyze the sequential circuit. Specifically, we will analyze the 2nd digit of the second hand and the first digit of the minute hand. For practical purposes, the tick frequency needs to be increased to 36 Hz.

After logging, we get the output file (Note: refer to the spreadsheet titled 'Output'):

In the header of the excel table, we have clock input, pause button, increase, and the outputs of each counter. When the pause is 0, the counters cycle through the designated binary numbers. The minute hand counter stays the same until the second-hand counter transitions from 101 to 000 (row 297). When pause is 1, none of the outputs in the counters change (row 146) unless "increase" is 1. We can successfully confirm that the inputs and outputs function as intended although there is always room for improvement.

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Discussion

Overall, the design worked the way I planned it to be but there could have been advancements and additions. One enhancement I could have made was to allow the user to increase their chosen value without sequentially affecting the other values. For example, the user can cycle through the counter 0-9 without the second digit counter increasing every 9 to 0 transition. One way this design could have been implemented was to use multiplexers on every clock output (which is rippled to all the counters) that will be enabled only if the user sends a signal using the 1:8 demultiplexer (Cycle feature). The parallel (where the input is a constant for the LEDs) 8:1 DMUX's outputs will be connected to the corresponding ENB input of the multiplexers.

One feature that should be added is AM/PM. This can be done using a counter that resets after 1 and is triggered when the 24-hour counter reaches binary 13.

There were choices that I considered during the process of designing. One of them was to use 5-bit adders and subtractors when converting to standard to military time. This will only require the 12-hour counter in the hour hand and AM/PM counter. The adder will add 12 if the counter is greater than 12 and PM. For example, 1 PM would be 13. To revert, subtract 12. However, 12 AM is 0 while 12 PM is 12. Due to the complexity of applying these conditions, I chose the design of the parallel counters.

This project helped me understand the fundamentals of digital electronics and the process of designing a device from the scratch. The design techniques learned in this course helped accelerate the completion of the project.